Amendments to the Claims

A complete list of pending claims follows, with indicated amendments:

1. (Amended) A debugging circuit capable of debugging a plurality of microprocessor sockets and any respective microprocessors included therein ~~possible microprocessors~~, comprising:

a debug port;

a plurality of microprocessor sockets, each of said microprocessor sockets adapted to receive a microprocessor;

a plurality of switches, each of said plurality of switches corresponding to a respective one of said plurality of microprocessor sockets;

wherein said plurality of microprocessor sockets are adapted to form a serial signal path, and wherein each of said switches is capable of automatically detecting whether a microprocessor is present in the corresponding microprocessor socket, and if a microprocessor is present in said corresponding microprocessor socket then said switch is automatically configured to include said microprocessor within said signal path, and if a microprocessor is not present in said corresponding microprocessor socket then said switch is automatically configured so that said signal path bypasses said corresponding microprocessor socket.

2. (Original) The debugging circuit according to claim 1, wherein a debugging input is provided to each microprocessor socket, and wherein a debugging output is provided from each microprocessor that is present in said corresponding microprocessor socket.

3. (Original) The debugging circuit according to claim 2, wherein each switch receives as an input a microprocessor detection signal indicating whether said corresponding microprocessor is present.

4. (Original) The debugging circuit according to claim 3, wherein for each switch, if said microprocessor is present then said switch provides as an output said debugging output of said corresponding microprocessor.

5. (Amended) The debugging circuit according to claim 4, wherein for each switch, if said microprocessor is not present, then said switch provides as a switch output said debugging input to said corresponding empty microprocessor socket.

6. (Original) The debugging circuit according to claim 5, wherein for each switch not corresponding to a last microprocessor in said serial signal path, said switch output is provided as a debugging input to a subsequent microprocessor in said serial signal path.

7. (Original) The debugging circuit according to claim 6, wherein for said switch corresponding to said last microprocessor in said serial signal path, said switch output is provided to said debug port.

8. (Original) The debugging circuit according to claim 7, wherein said debug port is electrically coupled to a computer and receives input from and provides output to said computer.

9. (Original) The debugging circuit according to claim 8, wherein said plurality of switches each comprise a pair of bipolar transistors.

10. (Original) The debugging circuit according to claim 8, wherein said plurality of switches each comprise field effect transistors.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Amended) A method for debugging at least one of a plurality of microprocessor sockets and any respective microprocessors included therein ~~possible microprocessors~~, comprising the steps of:

providing a debugging circuit having a plurality of microprocessor sockets adapted to form a serial signal path, wherein each microprocessor socket ~~corresponds to a different one of said plurality of possible microprocessors and~~ is capable of receiving a microprocessor;

providing a switch corresponding to each of said microprocessor sockets;

providing as an input to each of said switches a processor detection signal indicating whether a microprocessor is present in said corresponding microprocessor socket;

providing as an input to each of said switches a bypass signal associated with the corresponding microprocessor socket ~~processor debugging input for said corresponding microprocessor~~;

providing as an input to each of said switches a processor debugging output from said corresponding processor if said microprocessor is present in said corresponding microprocessor socket;

said switch providing as a switch output said bypass signal ~~processor debugging input~~ if said corresponding microprocessor is not present in said corresponding microprocessor socket, and providing as a switch output said processor debugging output if said microprocessor is present in said corresponding microprocessor socket.

18. (Amended) The method according to claim 17, further comprising the step of:

for each switch corresponding to a microprocessor socket that is not a last microprocessor socket in said serial signal path, providing said switch output as the ~~a~~ debugging input directed to a subsequent microprocessor socket in said serial signal path.

19. (Amended) The method according to claim 18, further comprising the step of:

for said switch corresponding to said last microprocessor socket in said serial signal path, providing said switch output to a debug port.

20. (Amended) The method according to claim 19, further comprising the step of:

providing as a debugging input directed to a first microprocessor socket in said serial signal path a signal received from said debug port.

21. (Original) The method according to claim 20, wherein said switches each comprise a pair of bipolar transistors.

22. (Original) The method according to claim 20, wherein said switches each comprise field effect transistors.

Remarks

Following the above amendments, claims 1-10 and 17-22 are pending in this application. The Examiner has rejected each of claims 1-10 and 17-22 on the grounds that these claims are obvious under 35 U.S.C. § 103 in view of allegedly admitted prior art in combination with U.S. Patent No. 5,706,447 to Vivio and U.S. Patent No. 6,249,832 to Sanders et al.

In addition, the Examiner has declared that the declaration is defective because it refers to joint inventors. The Examiner has also rejected claims 1, 5, and 17 under 35 U.S.C. § 112, second paragraph, for being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as his invention.